The ASDQ ASIC

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Abstract

The ASDQ ASIC provides eight channels of complete signal processing for the Central Outer Tracker (COT) being built for the CDF upgrade. The ASDQ has been fabricated using the well-characterized and radiation tolerant MAXIM SHPi analog bipolar process. It optimizes competing requirements of short measurement time ($\approx$ 7 ns), good double pulse resolution ($\approx$ 20 ns), low power (≈ 35 mW/ch) and low operational threshold ($\approx 2-3$ fC). It contains a low noise pseudo-differential preamplifier, ion tail compensation and multipole shaper, baseline restorer, comparator with an optional linear width encoded charge measurement and an on-chip calibration circuit. The design of the circuit is based on GARFIELD simulations of COT tracks and the response of a prototype chamber to Cosmic rays and Fe^{55} sources.

I. Introduction

The CDF collaboration is constructing the Central Outer Tracker (COT) for the 2000-2002 data taking run of the Tevatron. The COT will operate in a high luminosity environment with a maximum drift time of 100 ns and rates up to 5 MHz in its inner layers. The COT will have 30,240 active readout channels, which is the largest number ever assembled in a colliding beam configuration.

The ASDQ ASIC provides eight channels of full analog signal processing between the chamber and the TDC chip. It optimizes competing requirements of short measurement time ($\approx$ 7 ns), good double pulse resolution ($\approx$ 20 ns), low power (≈ 35 mW/ch) and low operational threshold ($\approx 2-3$ fC). The ASDQ ASIC measures 5.4 mm $\times$ 3.9 mm on the silicon substrate and has been fabricated using the well-characterized and inherently radiation tolerant MAXIM SHPi analog bipolar process. Each channel of the circuit contains about 800 hand placed custom components. The total number of active components on the chip is more than 6000.

II. ASDQ Overview

Figure 1 shows an ASDQ single channel block diagram. Each channel consists of a low noise preamplifier, ion tail compensation and multipole shaper, a baseline restorer and a discriminator with an optional linear width encoded charge measurement (dE/dx). The shaper allows good noise performance and double pulse resolution. The baseline restoration is implemented before the discriminator and allows high rate performance, insensitivity to mismatches in ion tail compensation and excellent chip to chip threshold uniformity. A

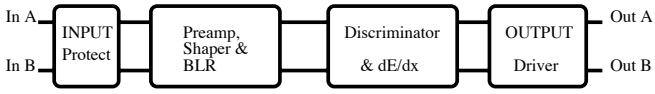

Figure 1: ASDQ single channel block diagram

measurment of charge is linearly encoded into the width of the comparator. Upon triggering the discriminator, the output of the baseline restoration is integrated onto a capacitor which is simultaneously discharged as it is integrating. The output of the discriminator is high while the voltage on the integrating capacitor is above the trailing edge threshold. The two parameters which determine the relationship between the discriminator output pulse width and the integrated charge are the trailing edge threshold and the capacitor drain current. A single programmable time over threshold discriminator based on the output of the baseline restorer is used when the charge measurement circuit is disabled.

Figure2 shows a SPICE simulation of the ASDQ response to a Cosmic ray event approximately equal to a radial track in the COT. From top to bottom the figure shows the input signal into the preamplifier, the output from the preamplifier, the output of the shaper, the output of baseline restoration and the output of the discriminator with charge measurement enabled and disabled.

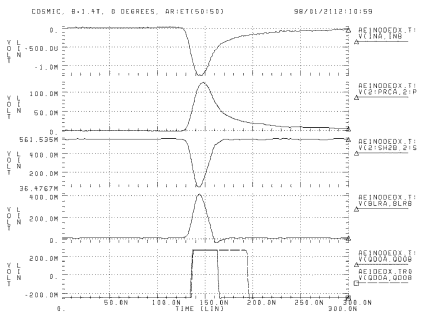

Figure 2: SPICE simulation of the ASDQ response to a Cosmic ray event.

The shaping and discriminator channels are fully differential while the preamplifier is pseudo-differential. This circuit technique provides excellent common mode noise rejection from the inputs through to the outputs and results in a symmetric and time-invariant current draw on the power supplies. A programmable on chip calibration circuit allows a determination of the relative t_0 and charge-to-width relation for each channel. The ASDQ also has a monitor point on the eighth channel which provides a buffered copy of the signal at the baseline

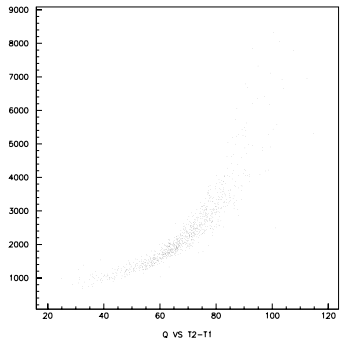

Figure 3: The expected integrated charge versus discriminator output pulse width from a GARFIELD simulation.

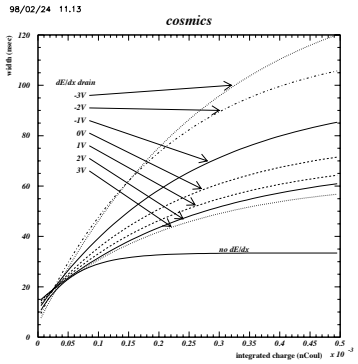

Figure 4: Fits to SPICE simulations of the discriminator output pulse widths as a function of the integrated charge.

restorer when enabled. This allows a study of the size and shape of the signal at that point in the circuit.

III. ASDQ CONTROLS

The ASDQ has a broad functionality integrated into the chip and offers multiple controls which allow adjustment of the discriminator thresholds and the charge encoded or time over threshold output widths. A single programmable threshold, based on the output of the baseline restorer, determines the leading edge trigger time for all channels independent of the charge measurement mode chosen. With the charge measurement enabled, the width of the output pulse can be adjusted using a programmable trailing edge threshold and drain current. A programmable $\times 2$ attenuator circuit can be used to reduce the amplitude of the output of the shaper into the baseline restorer.

IV. ASDQ DESIGN

The design of the ASDQ is driven by realistic simulations of COT tracks using GARFIELD. This CERN drift simulation package allows the study of charge deposition and arrival times in a drift cell. We have implemented a full modelling of the analog behavior of the various stages of the ASDQ. An analog simulation package designed at the University of Pennsylvania uses the output of GARFIELD to calculate the response of the ASDQ circuit to COT tracks. This allowed us to study the expected behavior of the ASDQ in realistic COT situations and to quantify the various design issues in shaping, baseline restoration, charge measurement and the various associated control voltages. This information was then used to optimize the design of the ASDQ. As a cross-check, we have also based the design on the response of a prototype chamber to Cosmic rays and Fe^{55} sources in order to optimize the performance of the circuit. The digitized output from a fast preamplifier connected the chamber was corrected to eliminate its dominant pole, compensated for preamplifier gain and fed into a SPICE model of the ASDQ. Figure 3 shows the expected integrated charge versus discriminator output pulse width

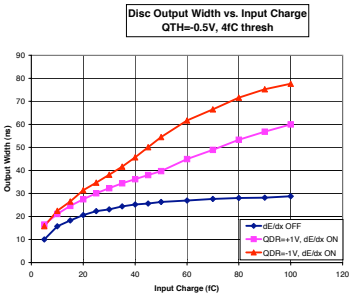

Figure 5: The measured discriminator output pulse widths as a function of the integrated charge.

from a GARFIELD simulation fed into a modelling of the response of the ASDQ.

V. ASDQ TESTS

Tests have been performed on the first prototype wafer received from the fabrication foundry. The functionality of the chip has been fully verified and is in good agreement with SPICE modelling. Figure 4 shows fits to SPICE simulations of the discriminator output pulse widths as a function of the integrated charge for different settings of the drain current. For comparison, figure 5 shows the measured discriminator output pulse widths as a function of the integrated charge for different settings of the drain current in fabricated ASDQ ASIC's. The yield based on one wafer is very high (90%). We have also observed a very good chip-to-chip and channel-to-channel uniformity in the response of the prototype ASDQ ASIC's.

VI. CONCLUSIONS

We have designed the ASDQ ASIC to provide full analog signal processing for the COT chamber. Full details of the circuit and its performance will be presented. General design methodology guided by physics measurement goals, experience with wire chamber ASIC's and the performance of the fabricated parts will be discussed.